REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1-20 under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Kluge (U.S. Patent Application No. 2003/183403) and Tsuji (U.S. Patent No. 5,901,023). The rejection has been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-20.

2. Claims 1-20 have been rejected under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Kluge (U.S. Patent Application No. 2003/183403) and Tsuji (U.S. Patent No. 5,901,023). The applicant respectfully disagrees with this rejection and the reasoning thereof.

In support of the rejection of claim 1, the Examiner states that Woo discloses parasitic capacitance to be a problem of concern when different RFIC sections are placed on separate power and ground lines, but does not disclose a first inductor assembly operably coupling the analog receive ground connection to the digital ground connection or a second inductor assembly operably coupling the analog transmit ground connection to the digital ground connection. However, Kluge discloses a parasitic capacitance 206 formed between an input terminal 203 and a ground terminal 204 in an RFIC having ESD protection, as well as the method of inserting an inductor 205 between the terminals in order to form a resonant tank with the parasitic capacitance 2006. The Examiner concludes that it would have been obvious to combine the method of inserting an inductor between tow terminals having a parasitic capacitance in between, as taught by Kluge, with the RFIC of Woo.

With reference to Figure 2a, Kluge teaches the use of an inductor 205 to provide the ESD protection for the terminal 203 when an ESD event occurs (paragraph 28) and the inductor 205 is sized to resonant with the parasitic capacitance 206 such that it does not impose a restriction with respect to the maximum processable frequency (paragraph 24).

With reference to Figure 3, Kluge teaches an integrated circuit 300 including an internal circuit 301 and an output stage 321. The IC 300 further includes a supply voltage terminal 302, a ground terminal 304, and a node 340 for an auxiliary voltage that is coupled to the supply voltage terminal 302 by a clamping element 307. The node 340 is also coupled to the ground terminal 304 by clamping element 308. The parasitic capacitances of the diodes 307 and 308 are indicated by reference numbers 309 and 310. An inductor 305 is coupled to the node 340 and to the output terminal 303. (paragraph 31) During normal operation, the inductor 305 provides a DC bias voltage from node 340 to the source of the transistor 321. In an embodiment, the inductor 305 is sized to resonate with the parasitic capacitance of the transistor 321. (paragraph 34) If an ESD event occurs, the current path is provided via the inductor and the diodes 307 and 308. The parasitic capacitance 309 and 310 of the diodes is relatively large, but because of the inductor 305, they do not adversely influence the output signal at terminal 303. (paragraph 35)

As such, Kluge is teaching that the inductor 205 or 305 is part of the ESD protection circuit, is coupled between the terminal to be ESD protected, and is coupled in parallel with the parasitic capacitance of a transistor to provide a parallel tank circuit during normal operation.

In contrast with Kluge, claim 1 claims, in part, first inductor assembly operably coupling the analog receive ground connection to the digital ground connection for ESD protection between analog and digital domains across the analog receive ground and digital ground connections; and second inductor assembly operably coupling the analog transmit ground connection to the digital ground connection for ESD protection between analog and digital domains across the analog transmit ground and digital ground connections.

Further, as taught in the specification of the present patent application on page 9, lines 25 – 28, inductors L1 and L2 are coupled between the ground connections 84, 86, and 88 to reduce the adverse affects caused by the parasitic capacitance and other

parasitic components of the ESD protection circuits 80 and 82 on the inbound RF signals 88 and the outbound RF signals 98. Still further, as shown in Figures 5 and 7 of the present patent application, the inductors are coupled essentially in series with the parasitics of the ESD circuits 80 and 82 forming a series LC circuit. As is known, a series LC circuit provides a low impedance at its resonant frequency and provides a high impedance outside of its resonant frequency. As is also known, a parallel tank circuit, as used in Kluge, provides a high impedance at its resonant frequency and provides a low impedance outside of its resonant frequency. As, such the parallel tank circuit of Kluge would provide the opposite desired effect as the series tank circuit of the embodiments of figures 2, 5, and 7.

Tsuji teaches placing resistors or transistors between analog ground and digital ground to provide ESD protection circuits and/or placing resistors or transistors between analog supply voltage and digital supply voltage for ESD protection circuits. ((Figures 1, 4, 5, and 6; column 1, line 64, - column 2, line 3; column 2, lines 14-19; and column 4, lines 14-19) As such, Tsuji is teaching the use of resistors or transistors between the analog and digital sections. In contrast, claim 1 now claims the inductors are used to reduce the adverse affects of the parasitic capacitance of the ESD circuits, not to be the ESD circuits as taught by Tsuji.

Based on the foregoing, the applicant believes that claim 1 overcomes the present rejection.

Claims 2-8 are dependent upon claim 1 and introduce additional patentable subject matter. The applicant believes that the reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claims 2-8 over the same rejection.

Claims 9 and 16 have been rejected for similar reasons as claim 1. Accordingly, the applicant believes that the reasons that distinguish claim 1 over the present rejection are applicable in distinguishing claims 9 and 16 over the same rejection.

Claims 10-15 are dependent upon claim 9, claims 17-20 are dependent upon claim 16, and each introduces additional patentable subject matter. The applicant believes that the reasons that distinguish claims 9 and 16 over the present rejection are applicable in distinguishing claims 10-15 and 17-20 over the same rejection.

For the foregoing reasons, the applicant believes that claims 1-20 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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